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(64) Apparatus for synchronization of a first signal with a second signal.

(57) Disclosed is an apparatus for synchronizing a first signal with a second signal comprising a plurality of delay means  $D_i$ , as  $i$  goes from 1 to  $N$ , where  $N$  is an integer, each delay means  $D_i$  having an input  $I_i$  and a delay output  $O_i$  for delaying a signal received at the respective input  $I_i$  by an increment  $\delta t$  of time in supplying the delayed signal at the respective delay output  $O_i$ .

The first delay means  $D_1$  of the plurality of delay means is connected to receive the first signal at its input  $I_1$ . Each of the other delay means  $D_i$ , for  $i$  equal to 2 to  $N$ , are connected in series such that the respective input  $I_i$  is connected to receive the delay output  $O_{i-1}$  of the preceding delay means  $D_{i-1}$ .

A plurality of latch means  $L_i$ , as  $i$  goes from 1 to  $N$ , are connected to be clocked by the second signal. Each of the latch means  $L_i$  latches the signal at the delay output  $O_i$  respectively for each of the delay means  $D_i$ , in response to the second signal and supplies the latched signal at a respective latch output  $Q_i$ .

Output logic means, responsive to at least a subset of the plurality of delay outputs  $O_i$  and plurality of latch outputs  $Q_i$ , for supplying essentially a phase-shifted copy of the first signal synchronized with the second signal is provided.

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APPARATUS FOR SYNCHRONIZATION OF A  
FIRST SIGNAL WITH A SECOND SIGNAL

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The present invention relates to apparatus for the synchronization of a first signal, such as a clock, with a second signal, such as an asynchronous external signal. The present invention has particular applicability in the field of synchronization of high-frequency clocks with asynchronous external signals.

In many applications it is necessary to synchronize an arbitrary first signal to a phase reference, such as an independently supplied second signal. In some cases this independently supplied second signal is a single "one-shot" signal, or occurs infrequently relative to the frequency of the first signal. For example, a high-speed video dot clock used in a high-resolution digital CRT display needs to be synchronized to the start of each video line. The start of each video line is identified by a line sync signal. However, this line sync signal may repeat only once for every thousand cycles of the video dot clock. Thus, for practical purposes, the line sync signal in this example is effectively an asynchronous single event.

The prior art accomplishes synchronization of a first signal with a second signal typically by one of two techniques. The first technique involves the use of a local clock having a frequency that is a large multiple of the frequency of the first signal, or clock, to be synchronized. The high-frequency multiple is supplied to a divider which is reset by the occurrence of the synchronizing second signal. The problem with this technique is the necessity of using a local clock having a much higher frequency than the frequency of the clock signal to be

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synchronized. Thus, for very high data frequencies, the cost of a local clock operating at large multiples of that high data frequency becomes prohibitive.

The second technique is the phase-locked loop frequency multiplier often used for systems having regularly spaced synchronizing signals. The phase-locked loop frequency multiplier operates by the use of a phase detector which detects the phase of the output of a divider that divides the frequency of the clock to be synchronized to match the frequency of the synchronizing signal and compares the divided output with the phase of the synchronizing signal. A phase correction signal is generated and supplied to a voltage-controlled oscillator which adjusts the clock to be synchronized to match the synchronizing signal. The clock signal output of the voltage-controlled oscillator is supplied to the divider which is fed back to the phase detector for comparison again with the synchronizing signal. Problems with phase-locked loop systems include the fact that it takes several synchronizing events for the phase-locked loop to lock up on the correct frequency. Also, phase-locked loops suffer stability problems when there are irregular or infrequent synchronizing events with respect to the frequency of the clock to be synchronized. In the high-frequency video dot clock example, discussed above, or other systems where the occurrence of the synchronizing signal might be considered an irregular or infrequent event, the phase-locked loop would be severely prone to degradation by jitter.

We will desire an apparatus for synchronizing a first signal with a second signal which eliminates the necessity of a clock generating a high-frequency multiple of the frequency of the signal to be synchronized. The apparatus avoids the stability and lock up problems of the phase-locked loop.

The apparatus for synchronizing a first signal with a second signal of the present invention comprises a plurality of delay means  $D_i$  as  $i$  goes from 1 to  $N$ , where  $N$  is an integer, each delay means  $D_i$  having an input  $I_i$  and a delay output  $O_i$  for delaying a signal received at the respective input  $I_i$  by an increment  $\delta t$  of time and supplying the delayed signal at the respective delay output  $O_i$ .

The first delay means  $D_1$  of the plurality of delay means is connected to receive the first signal at its input  $I_1$ . Each of the other delay means  $D_i$ , for  $i$  equal to 2 to  $N$ , are connected in series such that the respective input  $I_i$  is connected to receive the delay output  $O_{i-1}$  of the preceding delay means  $D_{i-1}$ .

A plurality of latch means  $L_i$ , as  $i$  goes from 1 to  $N$ , are connected to be clocked by the second signal. Each of the latch means  $L_i$  latches the signal at the delay output  $O_i$ , respectively for each of the delay means  $D_i$ , in response to the second signal and supplies the latched signal at a respective latch output  $Q_i$ .

Output logic means, responsive to at least a subset of the plurality of delay outputs  $O_i$  and plurality of latch outputs  $Q_i$ , for supplying essentially a phase-shifted copy of the first signal synchronized with the second signal is provided.

#### Brief Description of the Drawings

Fig. 1 is a logic diagram of one embodiment of the present invention.

Fig. 2 is a timing diagram used in the explanation of the apparatus of Fig. 1.

Fig. 3 is a logic diagram of an alternate embodiment of the present invention.

Fig. 4 is a timing diagram used in the explanation of the apparatus of Fig. 3.

### Detailed Description

With reference to the figures, a detailed description of the present invention is provided.

Fig. 1 shows an apparatus 10 for synchronizing a first signal  $S_1$  with a second signal  $S_2$  by generating an output signal  $S_0$  that is essentially a phase shifted copy of the first signal  $S_1$  synchronized with the second signal  $S_2$ .

The apparatus 10 includes a delay line 11 consisting of a plurality of delay means  $D_i$  as  $i$  goes from 1 to  $N$ . Each delay means  $D_i$  includes an input  $I_i$  and a delay output  $O_i$ . The delay means  $D_i$  delays the signal received at its respective input  $I_i$  by an increment  $\delta t$  of time and supplies the delayed signal at its respective delay output  $O_i$ . The first delay means  $D_1$  of the plurality of delay means in the delay line 11 is connected to receive the first signal  $S_1$  at its input  $I_1$ . Each of the other delay means  $D_i$ , for  $i = 2$  to  $N$ , are connected in series such that the respective input  $I_i$  is connected to receive the delay output  $O_{i-1}$  of the preceding delay means  $D_{i-1}$ . Thus, the output  $O_1$  of the first delay means  $D_1$  is supplied to the input  $I_2$  of the second delay means  $D_2$ . The output  $O_2$  of the second delay means  $D_2$  is connected to the input  $I_3$  of the third delay means  $D_3$  and so on. The delay means  $D_i$  may be implemented with buffers having a desired propagation delay so that the increment  $\delta t$  time meets a particular need.

Depending on the characteristics of the first signal  $S_1$  as discussed in more detail below, there may be additional delay means such as delay means 12 connected to receive the output  $O_N$  from the delay means  $D_N$ .

A plurality of latch means  $L_i$  as  $i$  goes from 1 to  $N$  are included. The latches are connected to receive respectively the delay output  $O_i$  from a corresponding delay means  $D_i$  as latch input, such as the D input of a D-type flipflop as shown in Fig. 1.

The second signal  $S_2$  is supplied at the clock input of each of the latch means  $L_i$  so that upon occurrence of the second signal  $S_2$ , the delay outputs  $O_i$  are latched by the

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latch means  $L_i$  and the latch means  $L_i$  supply latched delay outputs at the respective latch outputs  $Q_i$ .

An output logic means shown generally at 13, responsive to at least a subset of the plurality of delay outputs  $O_i$  and plurality of latch outputs  $Q_i$  across lines 14<sub>i</sub> and 15<sub>i</sub>, respectively, is included. The output logic means 13 supplies the output signal  $S_o$  which is essentially a phase shifted copy of the first signal  $S_1$  and synchronized with the second signal  $S_2$ .

The output logic means 13 in the embodiment shown in Fig. 1 includes a plurality of gate means  $G_i$ , for  $i = 1$  to  $N$ , each gate means  $G_i$  having a first input 16<sub>i</sub>, a second input 17<sub>i</sub> and a third input 18<sub>i</sub> and generates a high output when the first input is low, the second input is high and the third input is high.

For detecting a rising edge as shown, each gate means  $G_i$  is connected having its first input 16<sub>i</sub> connected to the latch output  $Q_k$ , where  $k = i + 1$  in the embodiment shown in Fig. 1 but can be any integer. The second input 17<sub>i</sub> is connected to receive latch output  $Q_l$  where  $l = i$  in the embodiment shown but can be any integer. The third input 18<sub>i</sub> is connected to the delay output  $O_j$ , where  $j = i$  in the embodiment shown in Fig. 1 but can be any integer. In order to detect a falling edge (not shown),  $k$  would equal  $i$ ,  $l$  would equal  $i + 1$  and  $j$  would equal  $i$  or another integer.

Output means 25, connected to receive the output 20<sub>i</sub> of each of the plurality of gate means  $G_i$  supplies the phase shifted copy of the first signal  $S_1$  as the output signal  $S_o$ . In the embodiment shown in Fig. 1 the output means 25 includes  $N$ -input OR-gate 19 having an output 21 and connected to receive as inputs the outputs 20<sub>i</sub> from each of the plurality of gate means  $G_i$  as  $i$  goes from 1 to  $N$ .

The operation of the apparatus 10 shown in Fig. 1 can be understood with reference to the timing diagram of Fig. 2. In Fig. 2, the signal  $S_1$  is shown as a periodic square

wave such as might be generated by high frequency clock. Signal  $S_1$  is supplied to the first delay means  $D_1$  and the output  $O_1$  as shown in Fig. 2 is a copy of the signal  $S_1$  shifted in time by an amount  $\delta t$ . The output  $O_1$  is supplied to the following input  $I_2$  and the output  $O_2$  of the second delay means  $D_2$  is shifted in time again by  $\delta t$  for a total shift of  $2\delta t$ .

Thus, following along the delay line 11 the output  $O_i$  will be a copy of the signal  $S_1$  shifted in time by an amount  $i \times \delta t$ , as shown in Fig. 2. Output  $O_{i+1}$  will be phase shifted copy of signal  $S_1$  but shifted in time by an amount  $(i+1) \times \delta t$ . The output  $O_N$  is a copy of the signal  $O_1$  but phase shifted by an amount  $N \times \delta t$  as shown in Fig. 2. In the preferred embodiment, the time  $N \times \delta t$  is at least as great as the period of the first signal  $S_1$  so that at any time that the second signal  $S_2$  may occur, the leading edge, or other characteristic of the first signal  $S_1$  to be detected as discussed below, will be located among the plurality of delay outputs  $O_i$ .

Assume the signal  $S_2$  occurs at a time  $i \times \delta t$  out of sync with the signal  $S_1$  as shown in Fig. 2. When the signal  $S_2$  occurs, the latches  $L_{i-y}$  through  $L_i$  will have a high signal at their respective inputs so the latch outputs  $Q_{i-y}$  through  $Q_i$  will be set high upon occurrence of the signal  $S_2$  where  $y$  is equal to or less than  $i$  and  $y \times \delta t$  is equal to or less than the length of the high portion of the first signal  $S_1$ . All of the following latch outputs  $Q_{i+1}$ ,  $Q_{i+2}$  through  $Q_{i+z}$  will latch a low output signal  $O_{i+1}$ ,  $O_{i+2}$  through  $O_{i+z}$  causing the latch outputs  $Q_{i+1}$ ,  $Q_{i+2}$  through  $Q_{i+z}$  to be low in this example where  $z$  is equal to or less than  $N$  and  $z \times \delta t$  is equal to or less than the length of the low portion of the signal  $S_1$ .

Thus the plurality of latch outputs  $Q_i$  identify the location of a characteristic of the first signal  $S_1$  among the delay outputs  $O_i$  upon the occurrence of the second signal  $S_2$ . In the embodiment shown in Fig. 2 the characteristic is the leading edge, or rising edge of the first

signal  $S_1$ . At the time of the second signal  $S_2$ , the rising edge of the signal  $S_1$  had propagated through  $i$  delay means, and upon occurrence of the second signal  $S_2$ , the plurality of latch means  $L_i$  will store data identifying the location of the leading edge of the signal  $S_1$  among the plurality of the delay outputs  $O_i$ .

The setting of the latch outputs  $Q_i$  enables the gate means  $G_i$  to supply the delay output  $O_i$  to the OR-gate 19 and through the OR-gate 19 as the output signal  $S_o$ . As can be seen, the first input on line 16<sub>i</sub> upon occurrence of the second signal  $S_2$  will be low because the latch output  $Q_{i+1}$  will be low. The second input on line 17<sub>i</sub> of the gate means  $G_i$  will be high because the latch output  $Q_i$  will be high. The third input 18<sub>i</sub> is connected to receive the delay output  $O_i$  and thus supplies the delay output  $O_i$  as the output to the gate  $G_i$ .

Only gate means  $G_i$  will be enabled to pass the delay output  $O_i$  through, while all other gate means will be disabled in the example shown. Thus the plurality of gate means  $G_i$  operate to detect the leading edge of the first signal  $S_1$  and select the delay output  $O_i$  that provides the proper phase shift  $i \times \delta t$  to the signal  $S_1$  in order to synchronize the signal  $S_1$  with the second signal  $S_2$ . The selected delay output  $O_i$  is supplied in the output signal  $S_o$ .

The output logic means 13 can be adapted to identify a wide variety of characteristics, the location of which will be identified by the plurality of latch outputs  $Q_i$ . For instance, many digital signals include start characters. The output logic means 13 could thus be adapted to identify the location of the start character among the latch outputs  $Q_i$  and select and supply the appropriate delay output  $O_i$  as the output signal  $S_o$  such that the output signal  $S_o$  synchronizes the start character or other characteristic of the first signal  $S_1$  with the occurrence of the second signal  $S_2$ .

The embodiment shown in Fig. 1 is operable in environments where the risk of metastable latch outputs  $Q_i$  is low. Further, the embodiment shown in Fig. 1 will generate an output signal  $S_0$  having a first cycle which is slightly distorted due to delays in the latch means  $L_i$  and the output logic means. For preventing problems due to metastable latch outputs and for obtaining maximum fidelity in the first cycle of the output signal  $S_0$ , the embodiment shown in Fig. 3 can be used.

Problems of metastable latch outputs occurs because when the second signal  $S_2$  clocks the plurality of latch means  $L_i$ , there is a possibility that the delay output  $O_i$  will be in transition thus causing an indeterminate input at the D-input to the latch means  $L_i$ . In this situation the latch output  $Q_i$  will be indeterminate but will settle at either a high or a low value.

The propagation delay is important only when it is desired to have maximum fidelity in the first cycle of the output signal  $S_0$ . For the purposes of the embodiment of Fig. 3, it is assumed that the propagation delay through the latch means  $L_i$  is approximately  $2 \times \delta t$ .

Fig. 3 shows an apparatus 10 for synchronizing a first signal  $S_1$  with a second signal  $S_2$  by generating an output signal  $S_0$  that is essentially a phase-shifted copy of the first signal  $S_1$  synchronized with the second signal  $S_2$ . The apparatus 10 includes a delay line 11. The delay line 11 includes a plurality of delay means  $D_i$  as  $i$  goes from 1 to  $N$ , only a portion of which are shown in Fig. 3.

Each of the delay means  $D_i$  generates a delay output  $O_i$  which is essentially a copy of the input to the delay means  $D_i$  phase shifted by an increment of time  $\delta t$ .

Each of the delay outputs  $O_i$  is supplied as an input to one of a plurality of latch means  $L_i$ , respectively. The latch means  $L_i$  are connected to be clocked by the second signal  $S_2$ . The latch outputs  $Q_i$  are set after a propagation delay of approximately  $2\delta t$ , in this example, after occurrence of the second signal  $S_2$ . In the embodiment

shown in Fig. 3, the latch means  $L_i$  are implemented using D-type flipflops.

The apparatus 10 includes an output logic means shown generally at 13, responsive to at least a subset of the plurality of delay outputs  $O_i$  and the plurality of latch outputs  $Q_i$  across lines  $14_i$  and  $15_i$ , respectively. The output logic means 13 supplies an output signal  $S_o$  which is essentially a phase-shifted copy of the first signal  $S_1$  and synchronized with the second signal  $S_2$ .

The output logic means 13 in the embodiment shown in Fig. 3 includes a plurality of gate means  $G_i$ , for  $i = 1$  to  $N$ , only a portion of which are shown in Fig. 3. Each gate means  $G_i$  has a first input  $16_i$ , a second input  $17_i$  and a third input  $18_i$ , and generates a high output when the first input is low, the second input is high and the third input is high.

The three inputs are connected as discussed above with reference to Fig. 1 such that its first input is connected to the latch output  $Q_k$ , where  $k = i + 2$ . The second input  $17_i$  is connected to receive latch output  $Q_l$  where  $l = i$ . The third input  $18_i$  is connected to the delay output  $O_j$  where  $j = i + 2$  in the embodiment shown in Fig. 3.

The output of each of the gates  $G_i$  is supplied to an output means 25, connected to receive each of the outputs from the plurality of gate means  $G_i$ , for supplying the phase-shifted copy of the first signal  $S_1$  as the output  $S_o$ . In the embodiment shown in Fig. 3 the output means 25 includes an N-input OR-gate 19 having an output 21 and connected to receive as inputs the outputs from the plurality of gate means  $G_i$ , as  $i$  goes from 1 to  $N$ .

The operation of the apparatus 10 shown in Fig. 3 can be understood with reference to the timing diagram of Fig. 4. As shown in Fig. 4, the delay output  $O_i$  is a phase-shifted copy of the first signal  $S_1$ . The delay output  $O_{i+2}$  is a phase-shifted copy of the delay output  $O_i$  having a shifted phase of approximately  $2 \times \delta t$ .

Assuming the second signal  $S_2$  occurs at the time the delay output  $O_i$  changes from low to high, then the plurality of latch means  $L_i$  will latch the delay outputs  $O_i$  such that the leading edge of the first signal  $S_1$  is identified as located at delay output  $O_i$ . Thus, the latch output  $Q_{i-1}$  after the propagation delay of  $2 \times \delta t$  will be set high. The latch output  $Q_i$  after the propagation delay will be set high. However, in case the delay output  $O_{i+1}$  happens to be in transition upon the occurrence of the second signal  $S_2$ , then the latch output  $Q_{i+1}$  will be indeterminate and eventually resolve to be either high or low as indicated in Fig. 4. Because of the propagation delay of the delay means  $O_i$ , the latch means  $L_{i+2}$  will latch a low signal so that the latch output  $Q_{i+2}$  will be low.

The embodiment shown in Fig. 3 accounts for the possibility that the latch output  $Q_{i+1}$  occurring close to the leading edge of the first signal  $S_1$  among the delay outputs  $O_i$  will be metastable. This is accomplished by connecting the first input  $16_i$  of the gate means  $G_i$  to the latch output  $Q_{i+2}$ . In this manner if the leading edge of the first signal  $S_1$  is occurring at the delay output  $O_i$ , then the gate means  $G_i$  will be enabled regardless of the possibility of metastable state of the latch output  $Q_{i+1}$ .

However, this also allows a second gate means, either  $G_{i-1}$  or  $G_{i+1}$  to be enabled. The consequences of this are discussed below.

The embodiment of Fig. 3 further provides for maximum fidelity of the output signal  $S_o$  in the first cycle of the output signal  $S_o$  by accounting for propagation delays in the latch means  $L_i$ . As discussed above, the propagation delay of  $2 \times \delta t$  is assumed for the embodiment of Fig. 3. Thus, in order to assure that the first cycle of the output signal  $S_o$  is as close to a true copy of the first signal  $S_1$  as possible, the third input  $18_i$  to the gate means  $G_i$  is connected to receive the delay output  $O_{i+2}$  for the entire series. For embodiments in which the latch means has a propagation delay that is close to an integer multiple  $X$  of

the time increment  $\delta t$ , then the third input  $18_i$  of the gate means  $G_i$  would be connected to receive the delay output  $O_{i+x}$ .

The output signal  $S_o$  which results from the embodiment of Fig. 3 is shown in the two possibilities labeled  $S_{o1}$  and  $S_{o2}$  in Fig. 4.

In the first case, the output signal  $S_{o1}$  is shown which would be generated in the event that the output  $Q_{i+1}$  settles at a high value. As shown, after the propagation delay of  $2 \times \delta t$ , the gate  $G_i$  and the gate  $G_{i+1}$  will be enabled to supply the delay outputs  $O_{i+2}$  and  $O_{i+3}$  (not shown) to the output OR-gate 19. Thus the signal  $S_{o1}$  in the first case will be the OR of delay output  $O_{i+2}$  and delay output  $O_{i+3}$ . Thus the leading edge 35 of the output signal  $S_{o1}$  will be determined by the delay output  $O_{i+2}$  while the falling edge 36 will be determined by the delay output  $O_{i+3}$ . This results in a slight distortion lengthening the high portion of the output signal  $S_{o1}$  of one delay increment  $\delta t$  at falling edge 36. However this is acceptable in embodiments in which  $\delta t$  is very small with respect to the frequency of the first signal  $S_1$ .

In the case in which the latch output  $S_{i+1}$  settles at a low value, the output signal resulting is shown as  $S_{o2}$  in Fig. 4. Upon the settling of the latch output  $Q_{i+1}$  to a low value, the gate means  $G_{i-1}$  and the gate means  $G_i$  will be enabled to supply at their respective outputs  $20_{i-1}$  and  $20_i$  the delay outputs  $O_{i+1}$  and  $O_{i+2}$  as inputs to the OR-gate 19. Thus the output signal  $S_{o2}$  will be the OR of delay outputs  $O_{i+1}$  and  $O_{i+2}$  so that the leading edge 37 in the second cycle of the output signal  $S_{o2}$  will be determined by the delay output  $O_{i+1}$ , while the falling edge 38 of the output signal  $S_{o2}$  will be determined by the delay output  $O_{i+2}$ . Because of the propagation delay of the latch means  $L_i$ , the leading edge of the output signal  $S_{o2}$  in the first cycle corresponds with the leading edge of the delay output  $O_{i+2}$ . Because both delay outputs  $O_{i+1}$  and  $O_{i+2}$  are tapped, the high time in the signal  $S_{o2}$  will be increased

by an amount  $\delta t$  at the leading edge. This distortion is tolerable in systems in which the increment  $\delta t$  is small with respect to the frequency of the first signal  $S_1$ .

In the embodiments shown in Fig. 1 and Fig. 3, when the characteristic of the first signal  $S_1$  to be detected occurs in two locations among the delay outputs  $O_i$ , then the first signal will be tapped at both locations. This will occur when two leading edges in the embodiments shown occur within the time interval  $N \times \delta t$  or the length of the delay line 11. When the first signal  $S_1$  is a clock or other waveform that repeats in each cycle, then the output signal so may distort in this instance by the resolution increment  $\delta t$  being added to the high time of the output signal  $S_o$ . If the first signal  $S_1$  is not a repetitive waveform, or one in which the mark to space ratio changes substantially from cycle to cycle, then the length of the delay line 11 should be adjusted to prevent the occurrence of two leading edges within the delay line, or the output logic means 13 should be adapted to detect the first occurrence.

In summary, the apparatus uses an asynchronous digital delay line 11 and a plurality of latch means  $L_i$  to capture a "snapshot" of the first signal  $S_1$  and then replay the first signal  $S_1$  in a phase determined by the "snapshot" which is locked to the synchronizing second signal  $S_2$ .

The resolution of the apparatus 10 according to the present invention is determined by the delay increment  $\delta t$  of each of the delay means  $D_i$ . With present ECL technology, buffers suitable for use as the delay means  $D_i$  can be fashioned having a propagation delay of about one nanosecond. The prior art is unable to accomplish resolution approaching that of the present invention without the use of a 1,000 megahertz clock.

The foregoing description of a preferred embodiment of the present invention has been presented for the purposes of illustration and description. It is not intended to be

exhaustive or to limit the invention to the precise form disclosed and obviously many modifications and variations are possible in light of the above teaching. The embodiments that identify a leading edge of the first signal and replay that signal beginning with that leading edge in synchronization with the second signal were chosen and described in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.

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CLAIMS

1. An apparatus for synchronizing a first signal with a second signal, comprising:

a plurality of delay means  $D_i$ , where  $i$  goes from 1 to  $N$  and  $N$  is an integer, each delay means  $D_i$  having an input  $I_i$  and a delay output  $O_i$  for delaying a signal received at the respective input  $I_i$  by an increment  $\delta t$  of time and supplying the delayed signal at the respective delay output  $O_i$ ;

one delay means  $D_1$  of said plurality of delay means having an input  $I_1$  connected to receive the first signal, and each of the other delay means  $D_i$  for  $i = 2$  to  $N$  being connected in series;

a plurality of latch means  $L_i$  where  $i$  goes from 1 to  $N$ , connected in communication with the second signal and the plurality of delay outputs  $O_i$ , each latch means  $L_i$  for latching the signal at the delay output  $O_i$ , respectively, in response to the second signal and for supplying the latched signal at latch output  $Q_i$ ; and

output logic means, responsive to at least a subset of the plurality of delay outputs  $O_i$  and plurality of latch outputs  $Q_i$ , for supplying essentially a phase-shifted copy of the first signal synchronized with the second signal.

2. The apparatus of Claim 1, wherein:

at least a subset of the plurality of latch outputs  $Q_i$  identify a characteristic of the first signal;

the output logic means includes means for detecting the characteristic of the first signal; and

selecting means, responsive to the means for detecting the characteristic, for selecting at least one of the plurality of delay outputs  $O_i$  and supplying the at least one selected delay output  $O_i$  as the phase-shifted copy of the first signal.

3. The apparatus of Claim 2, wherein the first signal has a leading edge and the characteristic detected is the location of the leading edge of the first signal among the latch outputs  $Q_i$ .

4. The apparatus of Claim 2, wherein the first signal includes a start character and the characteristic detected is the location of the start character among the latch outputs  $Q_i$ .

5. The apparatus of Claim 1, wherein said output logic means includes:

a plurality of gate means  $G_i$  for  $i = 1$  to  $N$ , each gate means  $G_i$  having a first input, a second input, and a third input, for generating a gate output in response to the first input, the second input and the third input;

each gate means  $G_i$  having its first input connected to latch output  $Q_k$ , where  $k$  is an integer, its second input connected to receive latch output  $Q_l$ , where  $l$  is an integer, and its third input connected to delay output  $O_j$ , where  $j$  is an integer; and

output means, connected to receive the gate output of each of the plurality of gate means  $G_i$ , for supplying the phase-shifted copy of the first signal.

6. The apparatus of Claim 5, wherein:

said output means includes an  $N$ -input OR-gate having an output and connected to receive the gate outputs from each of the plurality of gate means  $G_i$  as  $i$  goes from 1 to  $N$  for supplying the phase-shifted copy of the first signal at the OR-gate output.

7. The apparatus of Claim 5, wherein:

each of the latch means  $L_i$  has a propagation delay, the propagation delay being close to  $\delta t$  times an integer  $x$ ; and

$$j = i + x.$$

8. The apparatus of Claim 5, wherein:  
 $j = i$ ;  $k = i + 1$ ; and  $l = i$ .
9. The apparatus of Claim 5, wherein:  
 $j = i + 2$ ;  $k = i + 2$ ; and  $l = i$ .
10. The apparatus of Claim 5, wherein:  
 $j = i$ ;  $k = i$  and  $l = i + 1$ .
11. An apparatus for synchronizing a first signal with a second signal comprising:
  - a plurality of delay means  $D_i$ , where  $i$  goes from 1 to  $N$  and  $N$  is an integer, each delay means  $D_i$  having an input  $I_i$  and a delay output  $O_i$  for delaying a signal received at the respective input  $I_i$  by an increment  $\delta t$  of time and supplying the delayed signal at the respective delay output  $O_i$ ;
  - one delay means  $D_1$  of the plurality delay means having an input  $I_1$  connected to receive the first signal, and each of the other delay means  $D_i$  for  $i = 2$  to  $N$  being connected in the series;
  - a plurality of latch means  $L_i$  where  $i$  goes from 1 to  $N$ , connected in communication with the second signal and the plurality of delay outputs  $D_i$ ;
  - each latch means  $L_i$  for latching the signal at the delay output  $O_i$  respectively, in response to the second signal and for supplying the latched signal at latch output  $Q_i$ , wherein at least a subset of the plurality of latch outputs  $Q_i$  identify a characteristic of the first signal;
  - means for detecting the characteristic of the first signal; and
  - selecting means, responsive to the means for detecting the characteristic, for selecting at least one of the plurality of delay outputs  $O_i$  and supplying the at least one selected delay output  $O_i$  as essentially a phase-shifted copy of the first signal synchronized at the characteristic with the second signal.

12. The apparatus of Claim 11, wherein the first signal has a leading edge and the characteristic detected is the location of the leading edge of the first signal among the latch outputs  $Q_i$ .

13. The apparatus of Claim 11, wherein the first signal includes a start character and the characteristic detected is the location of the start character among the latch outputs  $Q_i$ .

14. An apparatus for synchronizing a first signal with a second signal comprising:

a plurality of delay means  $D_i$ , where  $i$  goes from 1 to  $N$  and  $N$  is an integer, each delay means  $D_i$  having an input  $I_i$  and a delay output  $O_i$  for delaying a signal received at the respective input  $I_i$  by an increment  $\delta t$  of time and supplying the delayed signal at the respective delay output  $O_i$ ;

one delay means  $D_1$  of said plurality of delay means having an input  $I_1$  connected to receive the first signal, and each of the other delay means  $D_i$  for  $i = 2$  to  $N$  being connected in series;

a plurality of latch means  $L_i$  where  $i$  goes from 1 to  $N$ , connected in communication with the second signal and the plurality of delay outputs  $O_i$ , each latch means  $L_i$  for latching the signal at the delay output  $O_i$ , respectively, in response to the second signal and for supplying the latched signal at latch output  $Q_i$ ;

a plurality of gate means  $G_i$  for  $i = 1$  to  $N$ , each gate means  $G_i$  having a first input, a second input, and a third input, for generating a gate output equal to the third input when the first input is low and the second input is high;

each gate means  $G_i$  having its first input connected to latch output  $Q_k$ , where  $k$  is an integer, its second input connected to receive latch output  $Q_1$  where 1

is an integer, and its third input connected to delay output  $O_j$ , where  $j$  is an integer; and

output means, connected to receive the gate output of each of the plurality gate means  $G_i$  for supplying essentially a phase-shifted copy of the first signal in synchronization with the second signal as an output signal.

15. The apparatus of claim 14, wherein:

said output means includes an N-input OR-gate having an output and connected to receive the gate outputs from each of the plurality of gate means  $G_i$  as  $i$  goes from 1 to N for supplying the phase-shifted copy of the first signal at the OR-gate output.

16. The apparatus of Claim 14, wherein:

each of the latch means  $L_i$  has a propagation delay, the propagation being close to  $\delta t$  times an integer  $x$ ; and

$$j = \text{to } i + x.$$

17. The apparatus of Claim 14, wherein:

$$l = i, k = i + 1 \text{ and } j = 1.$$

18. The apparatus of Claim 14, wherein:

$$l = i, k = i + 2 \text{ and } j = 1 + 2.$$

19. The apparatus of Claim 14, wherein:

$$j = i; k = i \text{ and } l = i + 1.$$

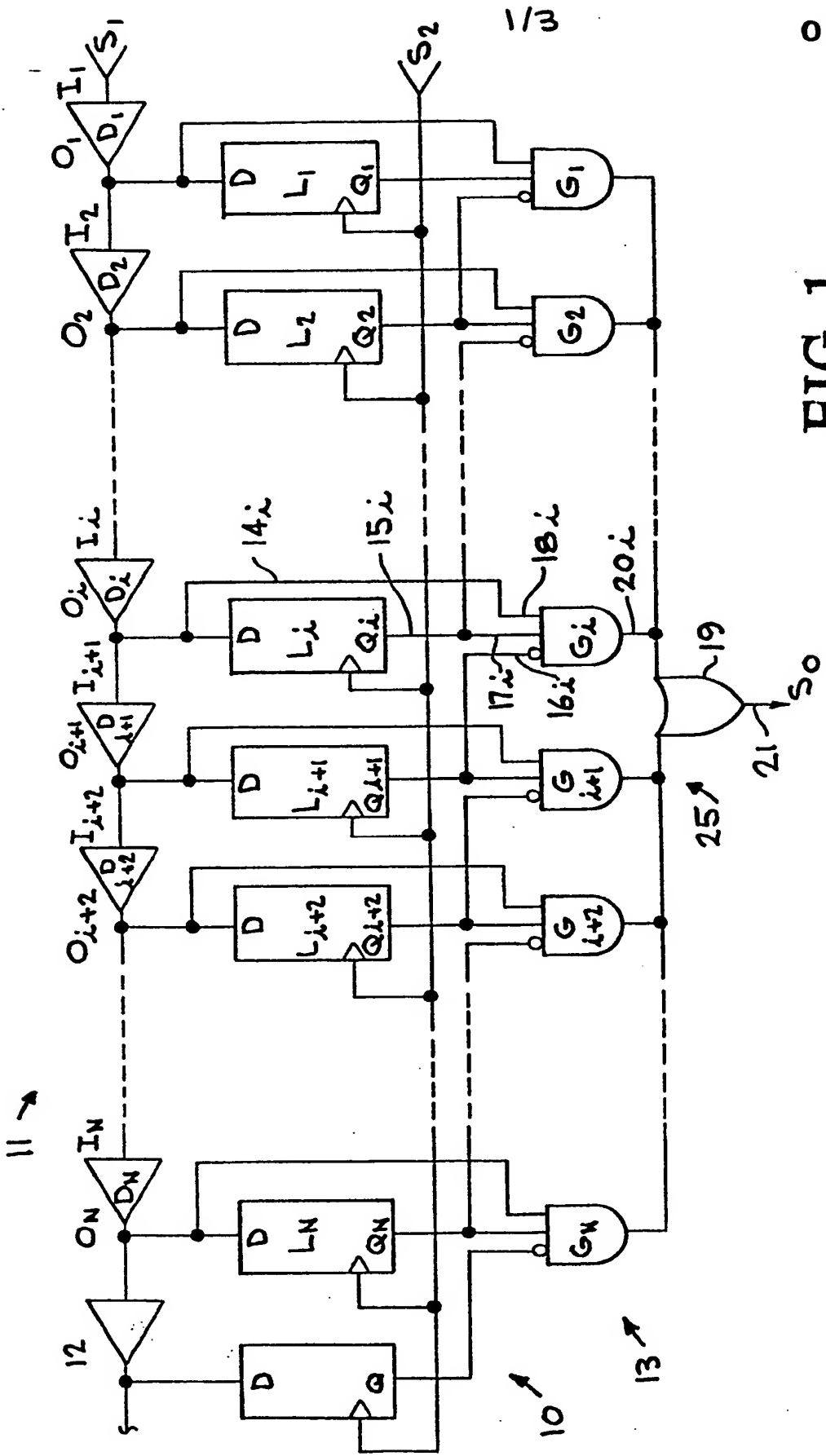


FIG. 1

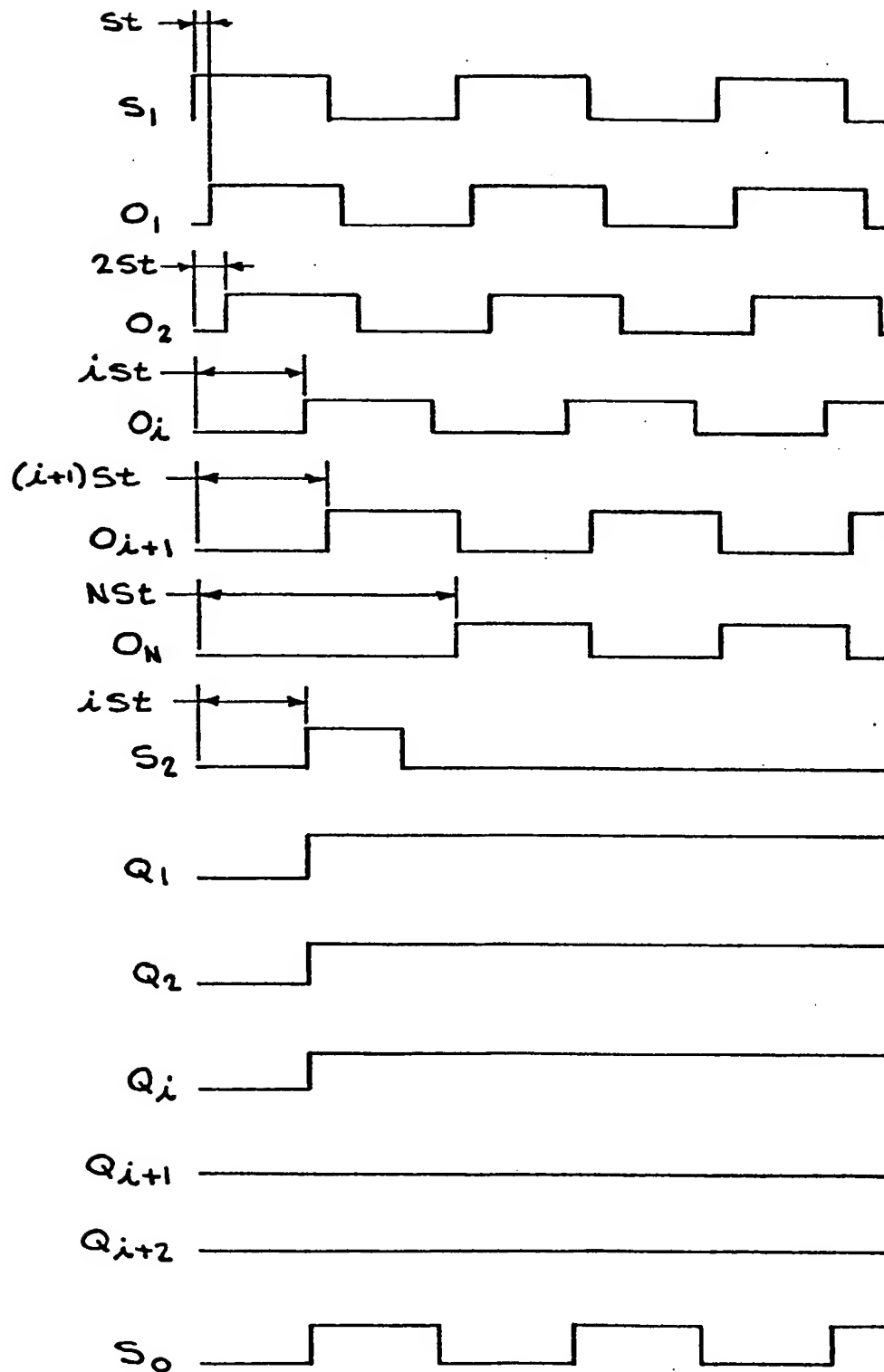


FIG. 2

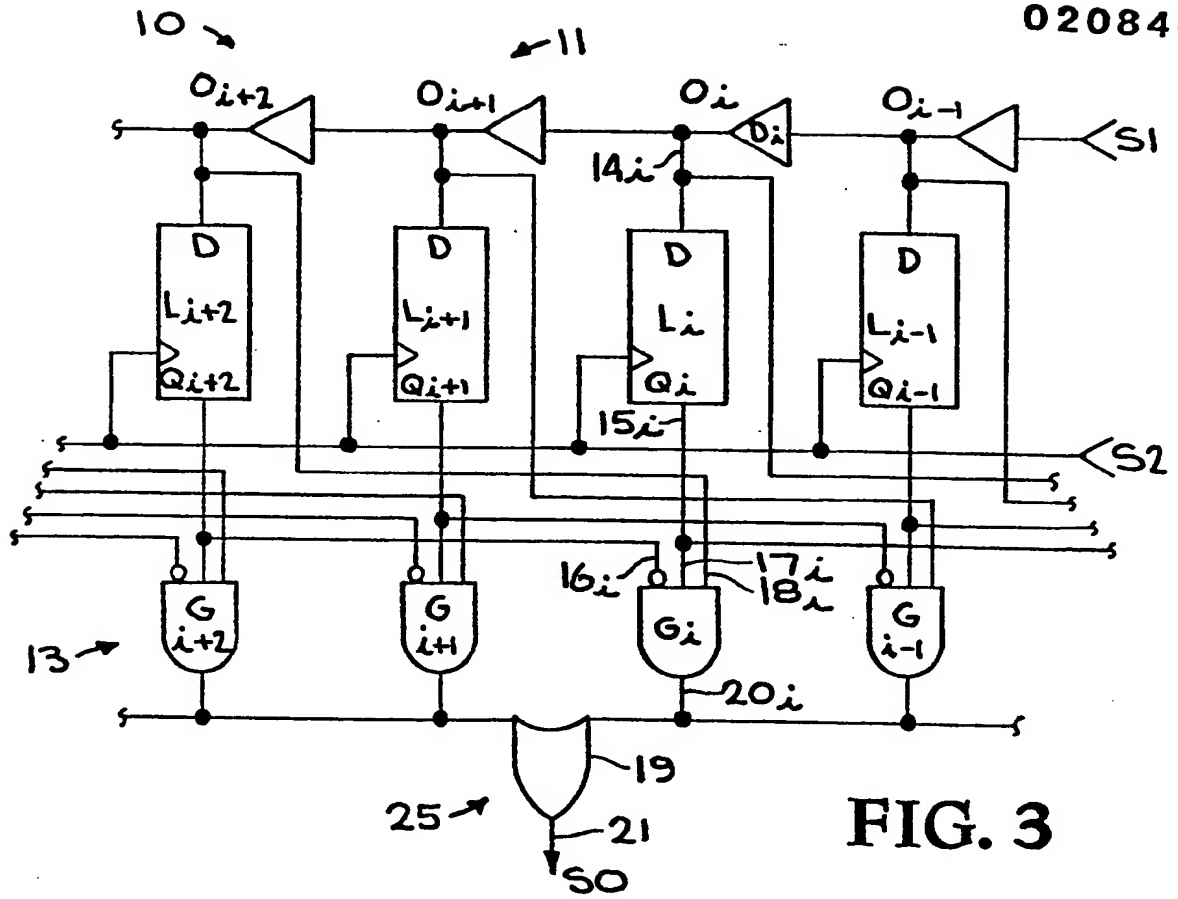


FIG. 3

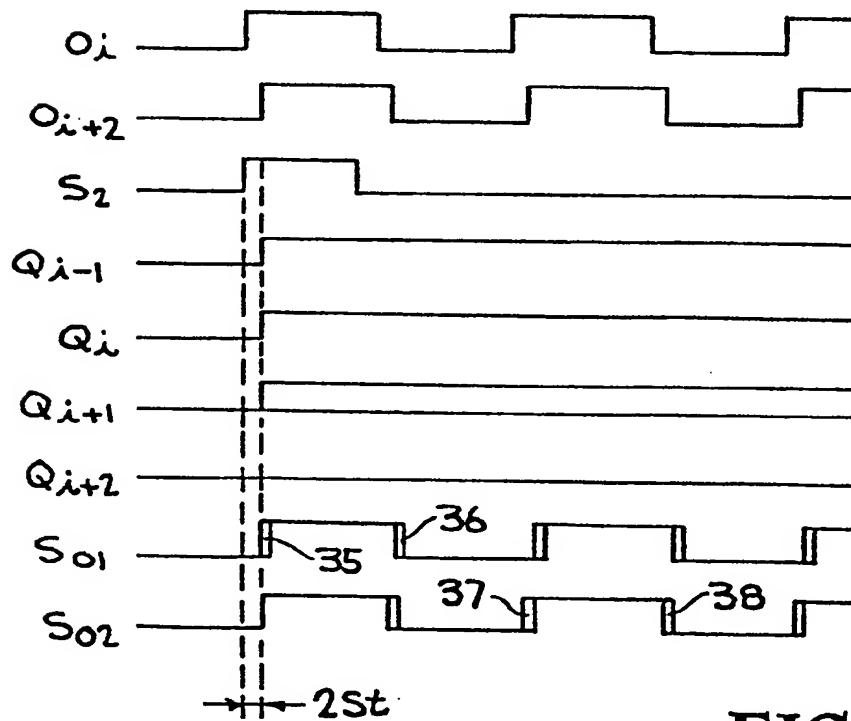


FIG. 4

(19)



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**Brookes & Martin 52/54 High Holborn**  
**London WC1V 6SE(GB)**(54) **Apparatus for synchronization of a first signal with a second signal.**

(57) Disclosed is an apparatus for synchronizing a first signal with a second signal comprising a plurality of delay means  $D_i$ , and  $i$  goes from 1 to  $N$ , where  $N$  is an integer, each delay means  $D_i$  having an input  $I_i$  and a delay output  $O_i$  for delaying a signal received at the respective input  $I_i$  by an increment  $\delta t$  of time in supplying the delayed signal at the respective delay output  $O_i$ .

The first delay means  $D_1$  of the plurality of delay means is connected to receive the first signal at its input  $I_1$ . Each of the other delay means  $D_i$ , for  $i$  equal to 2 to  $N$ , are connected in series such that the respective input  $I_i$  is connected to receive the delay output  $O_{i-1}$  of the preceding delay means  $D_{i-1}$ .

A plurality of latch means  $L_i$ , as  $i$  goes from 1 to  $N$ , are connected to be clocked by the second signal. Each of the latch means  $L_i$  latches the signal at the delay output  $O_i$  respectively for each of the delay means  $D_i$ , in response to the second signal and supplies the latched signal at a respective latch output  $Q_i$ .

Output logic means, responsive to at least a subset of the plurality of delay outputs  $O_i$  and plurality of latch outputs  $Q_i$ , for supplying essentially a phase-shifted copy of the first signal synchronized with the second signal is provided.

**EP 0 208 449 A3**



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# EUROPEAN SEARCH REPORT

Application Number

EP 86 30 4777

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y	GB-A-2 069 263 (PHILIPS) * Figure 1; page 1, line 86 - page 2, line 61 *	1-3	H 03 L 7/08 H 03 L 7/00
A	---	11,14	
Y	PATENT ABSTRACTS OF JAPAN, vol. 8, no. 226 (E-272)[1663], 17th October 1984; & JP-A-59 105 721 (MATSUSHITA DENKI SANGYO K.K.) 19-06-1984 * Abstract; figure *	1-3	
A	---	11,14	
A	GB-A-2 129 658 (TOKYO SHIBAURA DENKI K.K.)		
A,P	EP-A-0 165 498 (K.K. TOSHIBA)		
A	PATENT ABSTRACTS OF JAPAN, vol. 5, no. 74 (E-57)[746], 16th May 1981; & JP-A-56 24 843 (FUJITSU K.K.) 10-03-1981		
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 18, no. 10, March 1976, pages 3334-3337, New York, US; W.C. LEUNG: "Digital phase-locked loop circuit"		H 03 L H 04 L H 04 N
P,A	EP-A-0 157 701 (FUJITSU LTD)		
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 01-08-1988	Examiner PEETERS M.M.G.
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